LISTING OF PENDING CLAIMS

1. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus.

2. (original) The memory system of claim 1 further comprising:

a second memory component connected to the first address and control bus and to the first data bus.

3. (original) The memory system of claim 1 further comprising:

a second memory component connected to the first address and

control bus; and

a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and has a second data bus symbol time that is shorter than the first address and control bus symbol time of the first address and control bus.

4. (original) The memory system of claim 1 wherein a quotient of the first data bus symbol

time divided by the first address and control bus symbol time is less than or equal to 1/8.

5. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the first memory component;

a first clock signal conductor connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus and wherein the first address and control bus symbol time is shorter than a first clock signal cycle time of the first clock signal.

6. (original) The memory system of claim 5 further comprising:

a second memory component connected to the first address and control bus, to the first clock signal conductor, and to the first data bus.

7. (original) The memory system of claim 5 further comprising:

a second memory component connected to the first address and control bus and to the first clock signal conductor; and

a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and has a second data bus

symbol time that is shorter than the first address and control bus symbol time of the first address and control bus.

8. (original) The memory system of claim 5 wherein a first quotient of the first data bus symbol time divided by the first address and control bus symbol time is less than or equal to 1/8 and a second quotient of the first address and control bus symbol time divided by the first clock signal cycle time is less than or equal to 1/2.

9. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus and wherein the first data bus has a first data bus symbol time that is shorter than a first address and control symbol time of the first address and control bus.

10. (original) The memory system of claim 9 further comprising:

a second memory component connected to the first address and control bus; and

a second data bus connected to the first memory controller and to the second memory component, wherein the second memory component includes a second termination structure connected to the second data bus and wherein the first data bus symbol time is shorter than the first address and control bus symbol time of the first address and control bus.

11. (original) The memory system of claim 9 wherein the first memory controller includes a

third termination structure connected to the first data bus.

12. (original) The memory system of claim 9 wherein a quotient of the first data bus symbol time divided by the first address and control bus symbol time is less than or equal to 1/8.

13. (original) The memory system of claim 9 wherein a calibration process is used to adjust a first termination value of the first termination structure.

14. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the first memory component;

and a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus, wherein the first data bus uses differential signaling, and wherein the first address and control bus uses non-differential signaling.

15. (original) The memory system of claim 14 further comprising:

a second memory component connected to the first address and control bus; and

a second data bus connected to the first memory controller and to the second memory component, wherein the second memory component includes a second termination structure connected to the second data bus and wherein the second data bus uses differential signaling.

16. (original) The memory system of claim 14 wherein the first memory controller includes a third termination structure connected to the first data bus.

17. (original) The memory system of claim 14 wherein a calibration process is used to adjust a first termination value of the first termination structure.

18. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus.

19. (original) The memory system of claim 18 further comprising:

a second memory component connected to the first address and control bus and to the first data bus.

20. (original) The memory system of claim 18 further comprising:

a second memory component connected to the first address and control bus; and a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and wherein the second memory component accesses a second word stored in the second memory component, the second word being wider than a second data bus width of the second data bus.

21. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first data bus uses differential signaling.

22. (original) The memory system of claim 21 further comprising:

a second memory component connected to the first address and control bus; and

a second data bus connected the first memory controller and to the second memory component, wherein the first memory controller includes a second receive circuit having a second read timing adjustment subcircuit for adjusting a second adjustable read data sampling time point for second read data sampled from the second data bus and wherein the second data bus uses differential signaling.

23. (original) The memory system of claim 21 wherein a calibration process is used to adjust the first adjustable read data sampling time point.

24. (original) The memory system of claim 21 wherein the first memory controller contains a first transmit circuit having a first write timing adjustment subcircuit for

adjusting a first adjustable write data driving time point for first write data driven on the first data bus.

25. (original) A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller component includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first memory component includes a first termination structure connected to the first data bus.

26. (original) The memory system of claim 25 further comprising:

a second memory component connected to the first address and control bus; and

a second data bus connected to the first memory controller and to the second memory component, wherein the first memory controller includes a second receive circuit having a second read timing adjustment subcircuit for adjusting a second adjustable read data sampling time point for second read data sampled from the second data bus and wherein the second memory component includes a second termination structure connected to the second data bus.

27. (original) The memory system of claim 25 wherein a calibration process is used to adjust the first adjustable read data sampling time point.

28. (original) The memory system of claim 25 wherein the first memory controller includes a first transmit circuit having a first write timing adjustment subcircuit for adjusting a first adjustable write data driving time point for first write data driven on the first data bus.

29. (original) The memory system of claim 25 wherein the first memory controller includes a

third termination structure connected to the first data bus.